REMARKS

The Office Action of 09/07/06 has been carefully considered. Reconsideration and allowance in view of the following remarks is respectfully requested.

Claims 1, 3, 15, 16 and 18 were rejected as being anticipated by Higashida. Claims 4, 6, 7, and 9-14 were rejected as being unpatentable over Higashida in view of Biro. These rejections are respectfully traversed.

Higashida described an interleaving process as part of an ATM packet switch. A basic interleaving method is shown in Figure 17 of Higashida and described in column 20 thereof. The same basic method is described as part of the BACKGROUND of the present specification. An alternative method of interleaving is described in column 24 of Higashida and illustrated in Figure 23 thereof. In this alternative method, interleaving is performed twice in succession, using two separate memories, to improve error correction performance.

Higashida does not address the problem addressed by the present invention, namely reducing memory requirements for interleaving and de-interleaving. Furthermore, Higashida is not believed to teach or suggest the claimed features, including the feature that when plural data having been written into the memory are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, and on the other hand, when plural data having been written into the memory are read in a column direction, plural data which is the next to be written are sequentially written in the column direction. Note that this alternation of directions is with respect to the same memory, unlike the arrangement of Higashida Figure 23.

Favorable consideration is respectfully requested.

Respectfully submitted,

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